TEXAS INSTRUMENTS

THS4221EVM
THS4225EVM

User's Guide

April 2003 *High Performance Linear Products*

SLOU160

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the specified input and output ranges described in the EVM User's Guide.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Read This First

About This Manual

This user's guide describes the evaluation module (EVM) used to evaluate the THS4221 and THS4225 high-speed op amps, and includes a complete circuit description, schematics for devices under test, and bill of materials.

How to Use This Manual

This document contains the following chapters:

- Introduction and Description
- Using the THS4221 and THS4225 EVMs
- THS4221 and THS4225 EVM Applications
- EVM Hardware Description

Information About Cautions and Warnings

This book may contain cautions and warnings.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

Related Documentation From Texas Instruments

The URLs below are correct as of the date of publication of this manual. Texas Instruments applications apologizes if they change over time.

- THS4221, THS4225 data sheet (SLOS399)
- Application report, *PowerPAD™ Thermally Enhanced Package* (SLMA002)
  http://www−s.ti.com/sc/psheets/slma004/slma002.pdf
- Application report, *PowerPAD™ Made Easy* (SLMA004)
  http://www−s.ti.com/sc/psheets/slma004/slma004.pdf
- Application report, *Electrostatic Discharge (ESD)* (SSYA008)
  http://www−s.ti.com/sc/psheets/ssya008/ssya008.pdf
- Application report, *High-Speed Amplifier PCB Layout Tips* (SLOA102).

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This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

Electrostatic Sensitive Components

This EVM contains components that can potentially be damaged by electrostatic discharge, Always transport and store the EVM in its supplied ESD bag when not in use. Handle using an antistatic wristband. Operate on an anti-static work surface. For more information on proper handling, refer to SSYA008.

Trademarks

PowerPAD is a trademark of Texas Instruments.

Contents

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Chapter 1

Introduction and Description

These EVMs provide platforms for testing the THS4221 in the 5-pin SOT (DBV) package and the THS4225 in the 8-pin MSOP (DGN) package. They contain the high-speed op amp, a number of passive components, and various features and footprints that enable the user to experiment, test, and verify various operational amplifier circuit implementations.

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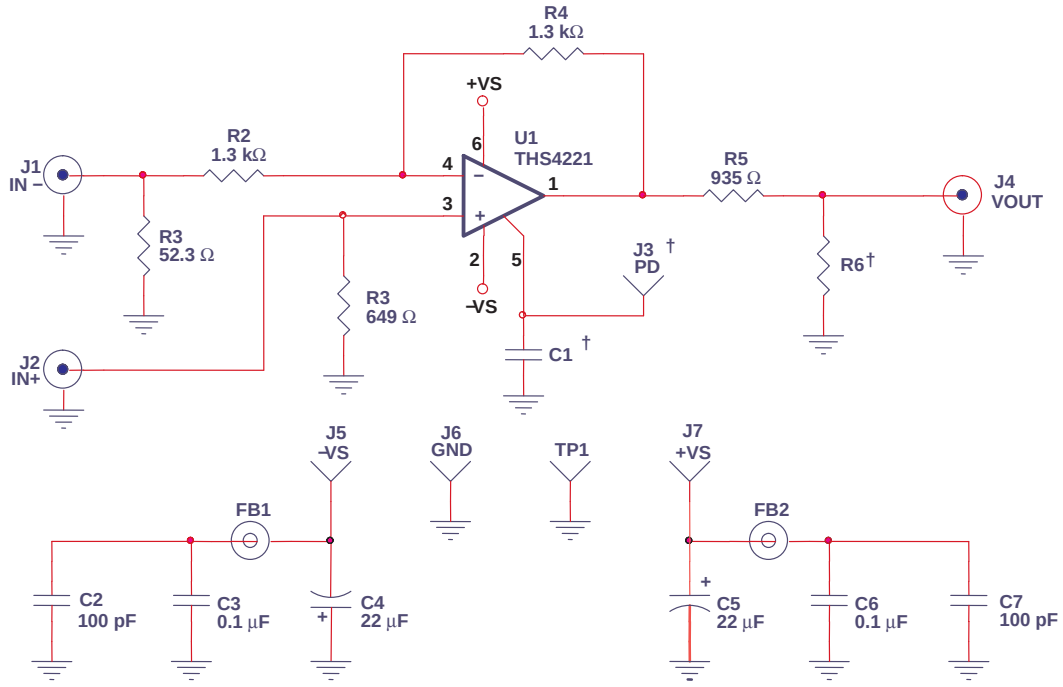
1.1 Evaluation Schematics

As delivered, the EVM has a fully functional example circuit; just add power supplies, a signal source, and monitoring instrument. See Figure 1−1 and Figure 1−2 for the default schematic diagrams. The user can change the gain by changing the ratios of the feedback and gain resistors (see the device data sheet for recommended resistor values). The EVM includes the following features:

- Wide operating supply voltage range: single supply 3 Vdc to dual supply ±7.5 Vdc operation (see the device data sheet). Single supply operation is obtained by connecting both GND and −VS to ground.
- Convenient GND test point (TP1).
- Power supply ripple rejection provided by inductors FB1 and FB2 followed by 22 µF capacitors.
- Decoupling capacitors on +VS and −VS populated with 0.1 µF and 100 pF.
- Nominal 50-Ω input impedance for the IN− inputs. Termination can be configured according to the application requirement.
- A good example of high-speed amplifier PCB design and layout. Also see High-Speed Amplifier PCB Layout Tips (SLOA102).
- 953-Ω resistors along with 50-Ω internal test equipment impedance provides minimum load of 1 kΩ.
- User customizable/configurable component choice.
- Nominal 50-Ω signal traces for input and outputs to reduce reduce signal reflections wiithin this board.
- PowerPAD™ heatsinking capability

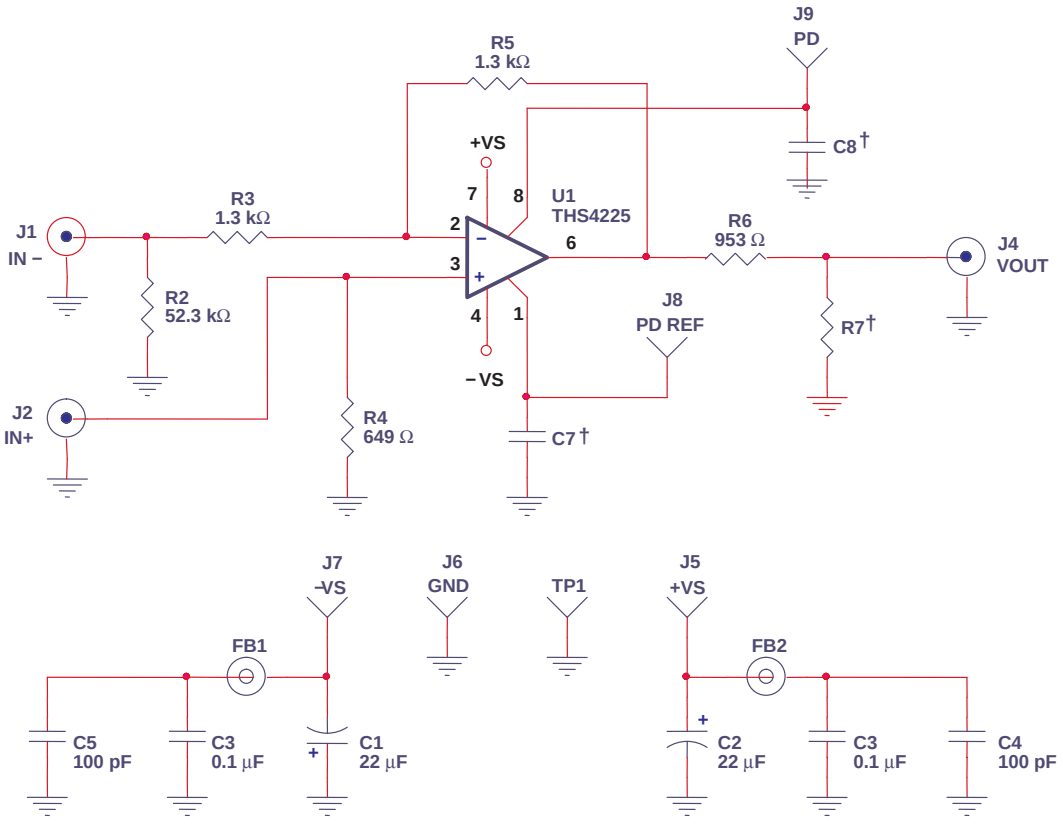
The default configuration for the EVM is designed to provide a 50-Ω terminated voltage gain of −1 with the amplifier loaded with approximately 1 kΩ. This voltage gain is the ratio of the voltage at the output pin of the amplifier (pin 1) to the voltage at the input at J1. The EVM also provides a nonterminated gain of 1.96 from the noninverting input connector J2 to the output pin of the amplifier (pin 1).

Figure 1−1. Schematic of the THS4221EVM



† Does not apply to the THS4221EVM

Figure 1−2. Schematic of the THS4225EVM



† Not installed on the THS4225EVM

Chapter 2

Using the THS4221 and THS4225 EVMs

This chapter shows how to connect the THS4221 and THS4225 EVMs to test equipment. It is recommended that the user connect the EVMs as shown in this chapter to avoid damage to the EVM or the devices installed on the board. Figure 2.1 shows how to connect power supplies, 50-Ω signal source, and 50-Ω monitoring instrument to a THS4221 EVM. Figure 2.2 shows how to connect power supplies, 50-Ω signal source, and 50-Ω monitoring instrument to a THS4225EVM.

Figure 2−1. THS4221EVM Connection Diagram

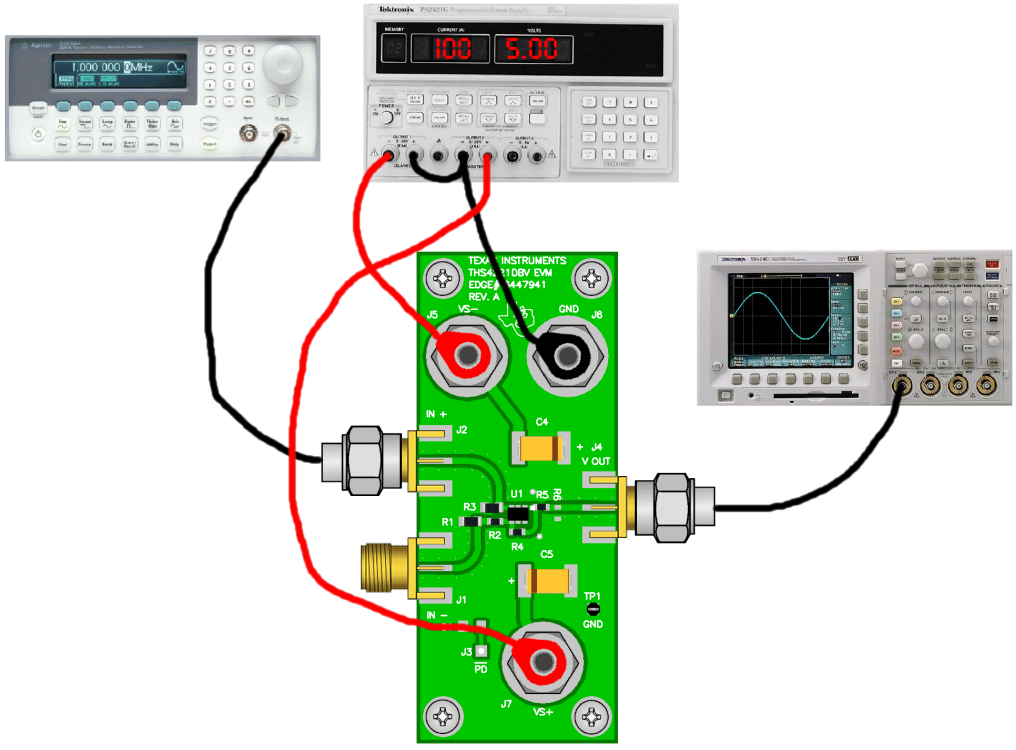


Figure 2−2. THS4225EVM Connection Diagram

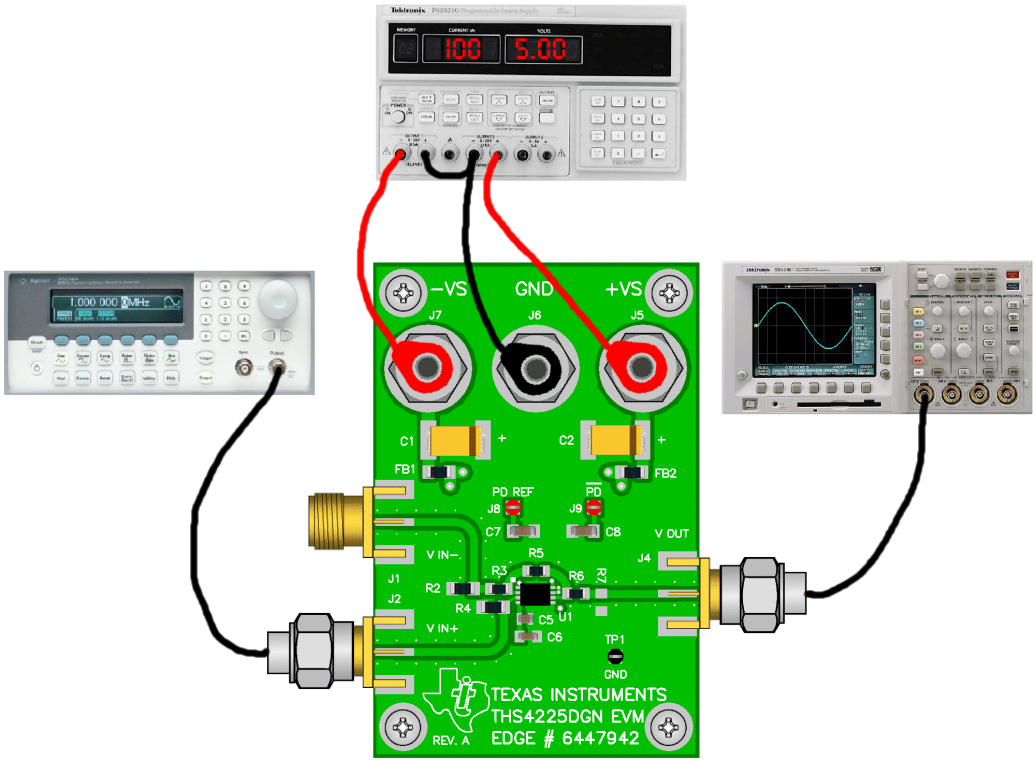


Figure 2−1 and Figure 2−2 show the connections to measure the output while a signal is inserted into the noninverting input of the EVM.

Chapter 3

THS4221 and THS4225 EVM Applications

Example applications are presented in this chapter. These applications demonstrate the most popular circuits to the user, but many other circuits can be constructed. The user is encouraged to experiment with different circuits, exploring new and creative design techniques. That is the function of an evaluation board.

Schematic diagrams and equations shown are for the THS4221 EVM, however it should be easy for the user to adapt the circuit and discussion for the THS4225 EVM.

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3.1 Inverting Video Gain Stage

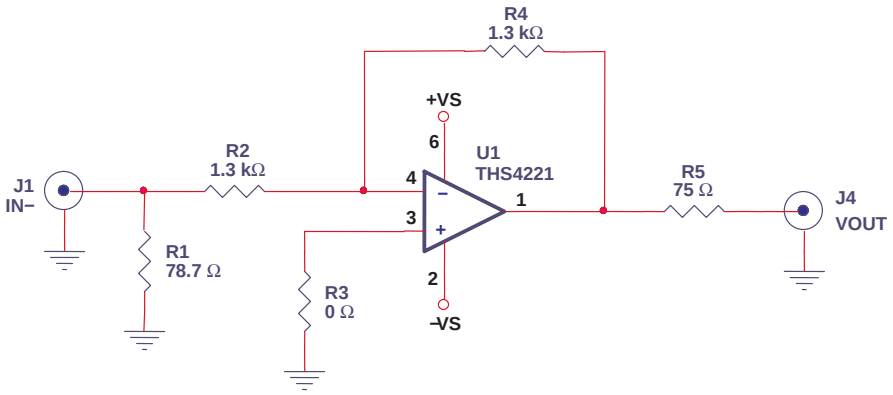
The circuit described in this section is an inverting gain stage with a voltage divider on the output, shown in Figure 3−1. The voltage gain from J1 to J4 is simplified in equation 1. Assuming a 75-Ω source impedance, equation 1 indicates the gain when R1 is changed to 78.7 Ω, and R3 and R5 are changed to 75 Ω. Rt is the termination resistance of the measurement device.

$$\frac{VOUT}{IN-} = \frac{R4}{R2}\left(\frac{Rt}{Rt + R5}\right) = -0.5 \quad (1)$$

R5 is used to match the output impedance of the amplifier to the line being driven and the instrument taking measurements. For short transmission line length, R5 can be replaced with a jumper.

R5 can also be used to isolate the amplifier from large capacitive loads.

Figure 3−1. Inverting Video Gain Stage

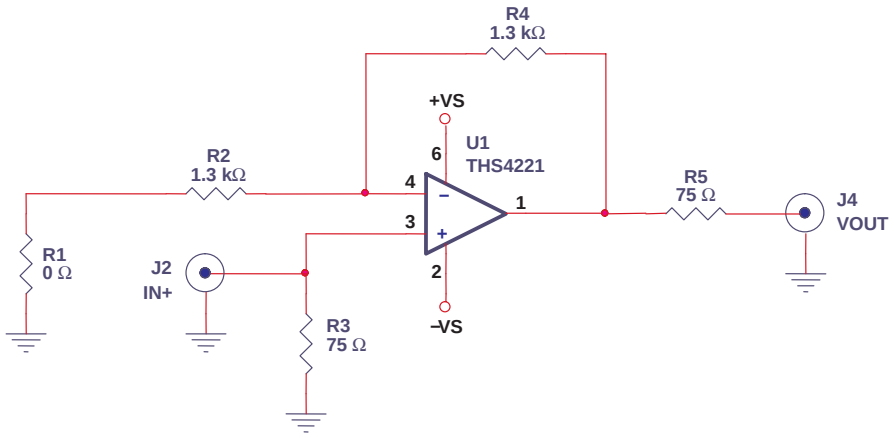


3.2 Noninverting Video Gain Stage

For a noninverting video gain stage, the EVM can be modified by replacing R1 with a 0 Ω resistor. A 75-Ω termination resistor is used in location R3 as shown in Figure 3−2. Equation 2 indicates the voltage gain from J2 to J4 when connected to a 75-Ω measurement instrument.

$$\frac{VOUT}{IN+} = \left(1 + \frac{R4}{R2}\right)\left(\frac{Rt}{Rt + R5}\right) = 1 \quad (2)$$

Figure 3−2. Noninverting Video Gain Stage



This is a common amplifier configuration used to drive transmission lines. The 75-Ω resistor in series with the output is for connection to a video instrument or circuit.

3.3 Power-Down Functionality Saves Power

The THS4225 EVM features a power-down pin (PD) which lowers the quiescent current from 14 mA down to 700 μA, ideal for reducing system power. The power-down pin of the amplifier defaults to the positive supply voltage in the absence of an applied voltage, putting the amplifier in the *power-on* mode of operation. To turn off the amplifier and conserve power, the power-down pin can be driven towards the negative rail. The threshold voltages for power-on and power-down are relative to the supply rails and given in the specification tables in the data sheets. Above the *Enable Threshold Voltage*, the device is on. Below the *Disable Threshold Voltage*, the device is off. Behavior in between these threshold voltages is not specified.

Note that this power-down functionality is just that; the amplifier consumes less power in power-down mode. The power-down mode is not intended to provide a high impedance output. In other words, the power-down functionality is not intended to allow use as a 3-state bus driver. When in power-down mode, the impedance looking back into the output of the amplifier is dominated by the feedback and gain setting resistors, but the output impedance of the device itself varies, depending on the voltage applied to the outputs.

The time delays associated with turning the device on and off are specified as the time it takes for the amplifier to reach 50% of the nominal quiescent current. The time delays are on the order of microseconds, because the amplifier moves in and out of the linear mode of operation in these transitions.

3.4 Power-Down Reference Pin Operation

In addition to the power-down pin, the THS4225 EVM features a reference pin (REF) which allows the user to control the enable or disable power-down voltage levels applied to the PD pin. Operation of the reference pin as it relates to the power-down pin is described below.

In most split-supply applications, the reference pin is connected to ground. In some cases, the user may want to connect it to the negative or positive supply rail. In either case, the user needs to be aware of the voltage level thresholds that apply to the power-down pin. The tables below show examples and illustrate the relationship between the reference voltage and the power-down thresholds.

Power-Down Threshold Voltage Levels (REF ≤ Midrail)			
Supply Voltage (V)	**Reference Pin Voltage (V)**	**Enable Level (V)**	**Disable Level (V)**
±5	GND	≥1.8	≤1
	−2.5	≥−0.7	≤−1.5
	−5	≥−3.2	≤−4
5	GND	≥1.8	≤1
	1	≥2.8	≤2
	2.5	≥4.3	≤3.5
3.3	GND	≥1.8	≤1

In the above table, the threshold levels are derived by the following equations:

REF + 1.8 V for enable

REF + 1 V for disable

Note that in order to maintain these threshold levels, the reference pin can be any voltage between Vs– or GND up to Vs/2 (midrail).

For 3.3-V operation, the reference pin must be connected to the most negative rail (for single supply this is GND).

Power-Down Threshold Voltage Levels (REF > Midrail)			
Supply Voltage (V)	**Reference Pin Voltage (V)**	**Enable Level (V)**	**Disable Level (V)**
±5	Floating or 5	≥4	≤3.5
	2.5	≥0.5	≤1
	1	≥0	≤−0.5
5	Floating or 5	≥4	≤3.5
	4	≥3	≤2.5
	3.5	≥2.5	≤2
3.3	Floating or 3.3	≥2.7	≤1.8

In the above table, the threshold levels are derived by the following equations:

REF − 1 V for enable

REF − 1.5 V for disable

Note that in order to maintain these threshold levels, the reference pin can be any voltage between (Vs+/2) + 1 V to Vs+, or left floating. The reference pin is internally connected to the positive rail, therefore it can be left floating to maintain these threshold levels.

For 3.3-V operation, the reference pin must be connected to the positive rail or left floating.

The recommended mode of operation is to tie the reference pin to midrail, thus setting the threshold levels to midrail +1.0 V, and midrail +1.8 V.

Chapter 4

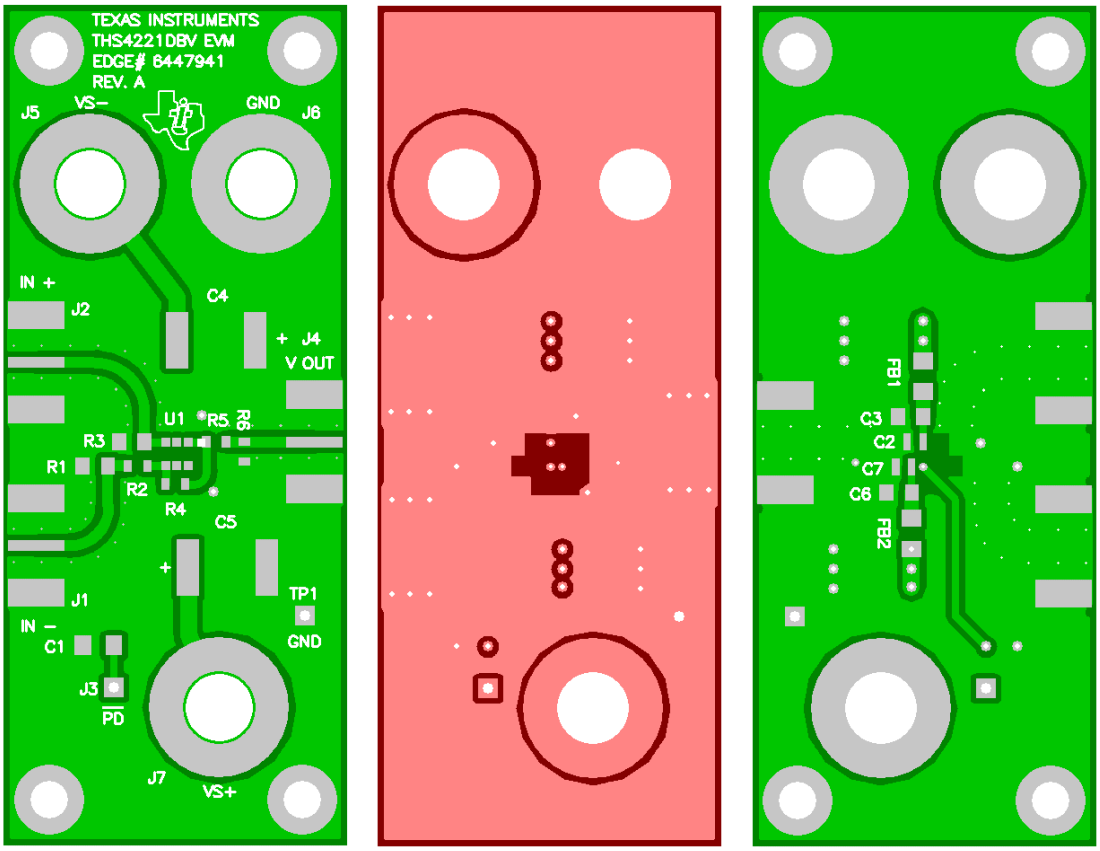
EVM Hardware Description

This chapter describes the EVM hardware. It includes the EVM parts list, component placement diagram and printed circuit board layout.

Table 4−1. THS4221EVM Bill of Materials

Item	Description	SMD Size	Ref. Des.	PCB Qty.	Manufacturer's Part No.	Distributor's Part No.
1	Bead, ferrite, 3A, 80 Ω	1206	FB1, FB2	2	(Steward) HI1206N800R-00	(Digi−Key) 240-1010-1-ND
2	OPEN	1206	C1	1		
3	CAP, 22 µF, tantalum, 25V, 10%	D	C4, C5	2	(AVX) TAJD226K025R	(Garrett) TAJD226K025R
4	CAP, 0.1 µF, ceramic, X7R, 50V	0805	C3, C6	2	(AVX) 08055C104KAT2A	(Garrett) 08055C104KAT2A
5	Cap, 100 pF, ceramic, 5%, 150 V	AQ12	C2, C7	2	(AVX) AQ12EM101JAJME	(TTI) AQ12EM101JAJME
6	OPEN	0603	R6	1		
7	Resistor, 1.3 kΩ, 1/10W, 1%	0603	R2, R4	2	(Phycomp) 9C06031A1301FKHFT	(Garrett) 9C06031A1301FKHFT
8	Resistor, 953 Ω, 1/10W, 1%	0603	R5	1	(Phycomp) 9C06031A9530FKRFT	(Garrett) 9C06031A9530FKRFT
9	Resistor, 52.3 Ω, 1/8W, 1%	0805	R1	1	(Phycomp) 9C08052A52R3FKHFT	(Garrett) 9C08052A52R3FKHFT
10	Resistor, 649 Ω, 1/8 W, 1%	0805	R3	1	(Phycomp) 9C08052A6490FKHFT	(Garrett) 9C08052A6490FKHFT
11	Jack, banana receptance, 0.25" diameter hole		J5, J6, J7	3	(HH Smith) 101	(Newark) 35F865
12	OPEN		J3	1		
13	Test point, black		TP1	1	(Keystone) 5001	(Digi-Key) 5001K-ND
14	Connector, edge, SMA PCB jack		J1, J2, J4	3	(Johnson) 142−0701−801	(Newark) 90F2624
15	IC, THS4221		U1	1	(TI) THS4222DBV	
16	Printed-circuit board			1	(TI) EDGE # 6447941 Rev.A	

Figure 4−1. THS4221EVM Board Layout Views

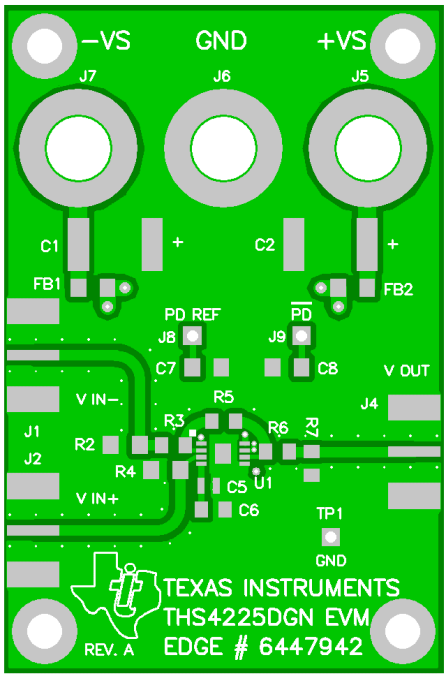


Layer 1: Top **Layers 2 and 3: Ground** **Layer 4: Bottom**

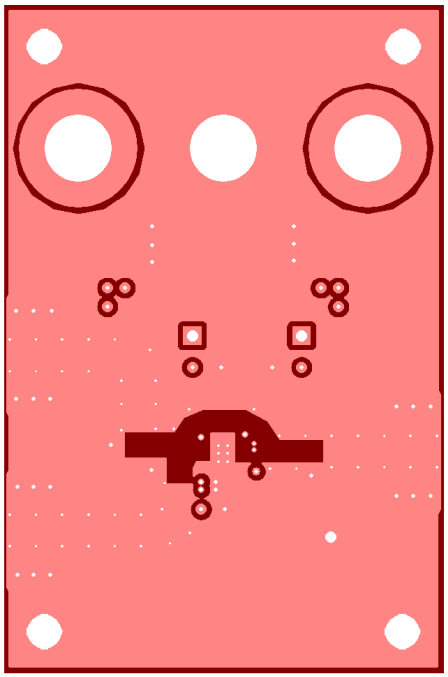
Table 4−2. THS4225EVM Bill of Materials

Item	Description	SMD Size	Ref. Des.	PCB Qty.	Manufacturer's Part No.	Distributor's Part No.
1	Bead, ferrite, 3A, 80 Ω	1206	FB1, FB2	2	(Steward) HI1206N800R-00	(Digi−Key) 240-1010-1-ND
2	CAP, 22 µF, tantalum, 25V, 10%	D	C1, C2	2	(AVX) TAJD226K025R	(Garrett) TAJD226K025R
3	Cap, 100 pF, ceramic, 5%, 150 V	AQ12	C4, C5	2	(AVX) AQ12EM101JAJME	(TTI) AQ12EM101JAJME
4	CAP, 0.1 µF, ceramic, X7R, 50V	0805	C3, C6	2	(AVX) 08055C104KAT2A	(Garrett) 08055C104KAT2A
5	CAP, 0.1 µF, ceramic, X7R, 50V	1206	C7, C8	2	(AVX) 12065C104KAT2A	(Garrett) 12065C104KAT2A
6	OPEN	0805	R7	1		
7	Resistor, 1.3 kΩ, 1/8W, 1%	0805	R3, R5	2	(Phycomp) 9C08052A1301FKHFT	(Garrett) 9C08052A1301FKHFT
8	Resistor, 953 Ω, 1/8W, 1%	0805	R6	1	(Phycomp) 9C08052A9530FKHFT	(Garrett) 9C08052A9530FKHFT
9	Resistor, 52.3 Ω, 1/4W, 1%	1260	R2	1	(Phycomp) 9C12063A52R3FKHFT	(Garrett) 9C12063A52R3FKHFT
10	Resistor, 649 Ω, 1/4 W, 1%	1260	R4	1	(Phycomp) 9C12063A6490FKHFT	(Garrett) 9C12063A6490FKHFT
11	Test point, black		TP1	1	(Keystone) 5001	(Digi-Key) 5001K-ND
12	Test point, red		J8, J9	2	(Keystone) 5000	(Digi-Key) 5000K-ND
13	Jack, banana receptance, 0.25" diameter hole		J5, J6, J7	3	(HH Smith) 101	(Newark) 35F865
14	Connector, edge, SMA PCB jack		J1, J2, J4	3	(Johnson) 142−0701−801	(Newark) 90F2624
15	Standoff, 4-40 hex, 0.625" length			4	(Keystone) 1808	(Newark) 89F1934
16	Screw, Phillips, 4-40, 0.250"			4	SHR-0440-016-SN	
17	IC, THS4221		U1	1	(TI) THS4225DGN	
18	Printed-circuit board			1	(TI) EDGE # 6447942 Rev.A	

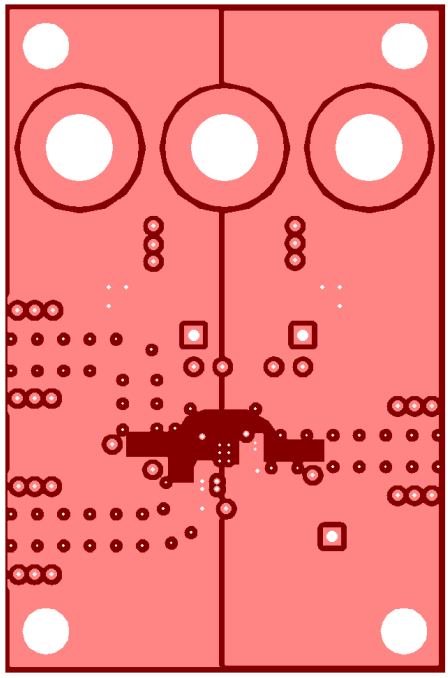
Figure 4−2. THS4225EVM Board Layout Views



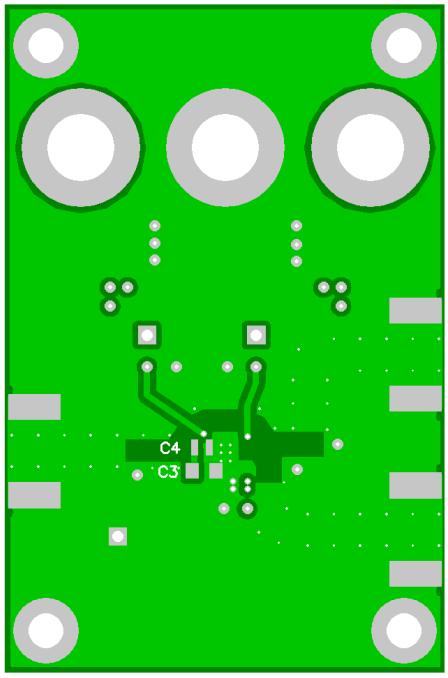
Layer 1: Top



Layers 3: Ground



Layer 3: Power



Layers 4: Bottom